REMARKS

The application has been amended so as to place it in condition for allowance at the time of the next Official Action.

Claims 1-9, 12-14, and 18-25 are pending. This amendment cancels claim 17, amends claims 1, 8, and 14, and adds new claims 18-25.

The specification has been amended as to form.

The Official Action rejected claim 14 under §112, first paragraph.

This claim has been amended so as to remedy the stated basis of rejection. More specifically, the claim now recites that the fixed end of the leads include a portion shaped to receive by direct contact, a corresponding one of a plurality of solder balls of a semiconductor chip. The claim further recites that the other end of the plurality of leads is shaped to contact with a corresponding one of a plurality of contact pads of a wiring substrate. With these amendments, it is clear that only the insulating sheet is being recited.

See further that the claim now recites that the portion shaped to receive by direct contact a corresponding one of the solder balls is in contact with the first surface of the insulating sheet.

Support for these recitations can be found at least in the drawing figures, see especially drawing Figure 2.

Withdrawal of the §112, first paragraph rejection is respectfully requested.

The Official Action rejected claim 17 under §112, second paragraph, as being incomplete. This claim has been canceled without prejudice.

The Official Action rejected claims 12-13 under §102 as being anticipated by KITAHARA 5,440,452.

The Official Action rejected claims 1-9 and 14 under §103 as obvious over KITAHARA in view of MIYAZAKI et al. 6,342,726.

At least as to dependent claim 14, see that the recited structure includes a portion in contact with the first (upper) surface, the portion being shaped to receive by direct contact a corresponding one of the solder balls. The KITAHARA reference does not make this disclosure. In the KITAHARA reference, the portion that directly receives the "solder balls" of chip 1 extends into the open interior of the insulating tape 4 (Figure 16).

In the present invention, an insulating sheet is provided for semiconductor chips with solder balls arranged to be lattice-like on the surface of the semiconductor chip (see lines 14-17 at page 6 in the specification), which is generally called BGA (Ball Grid Array). In BGA technology, conventionally the semiconductor chip is directly mounted on the wiring substrate (see lines 11-21 at specification page 1), and the resin is

filled into a gap between the chip. This resin includes both the solder balls and the wiring substrate, as illustrated by prior art Figure 7 of the present application. This prior art insertion of resin makes it difficult to detach the semiconductor from the wiring substrate at a later point in time because the space between the substrate and the lower surface of the semiconductor chip is filled with resin.

A feature of the present invention is an insulating sheet with leads in BGA technology which eliminates the necessity to cover the solder balls with resin. With such an insulating sheet, the semiconductor chip can be detached from the wiring substrate.

The insulating sheet, wherein the holes are arranged in a grid array as per claim 1, is not taught or suggested by the applied reference.

The Official Action stated that KITAHARA disclosed the entire recited invention with the exception of the connection bumps of the chip being solder balls. For this feature, the Official Action offers MIYAZAKI.

This proposed modification of KITAHARA is not believed to be viable. The Official Action does not take into account that the contact points between the taped carrier package leads and the semiconductor chip are not in contact with the insulation sheet itself, but rather flex over an opening within the insulating sheet. The Official Action has not considered how

using solder balls would work with such a tape carrier package structure. Accordingly, it is not evident that the proposed modification would be successful as required to make a viable obviousness rejection.

Further, independent claim 1 has been amended to recite that the solder balls of the semiconductor chip are arranged in a grid array. The tape carrier package of KITAHARA does not accommodate a semiconductor chip with the solder balls arranged in a grid array. Accordingly, the reference can neither anticipate nor render obvious the amended claim 1 recitation.

Furthermore, see that a recited feature of claims 3 and 12 is that one end of each lead is fixed on a first surface of the insulating sheet while the other end of each lead is shaped to be afloat in a corresponding one of the holes. As noted above, the first end (corresponding to the portion which would come in contact with the semiconductor chip) is not fixed on a first surface of the insulating sheet in the applied reference. Rather, the applied reference teaches the first end extending into a central hole portion of the carrier tape package.

Additionally, the applied reference does not teach that the other end of each of the leads being shaped to be afloat in the holes. Rather, the applied reference teaches the end 33 (Figure 16) being in contact with the tape carrier package peripheral portion. See that it is a central region 32 of the

lead (and not an end) that is intended to contact electrical connection 72 of element 7 in Figure 16.

Thus, contrary to that recited, in KITAHARA, leads 3 bridge a window 44 as shown in Figures 2 and 14. The outer end 33 of each lead, which is corresponding to the outer end 12 of the present invention, is fixed to the support film 4 (see column 5, lines 52-54, as well as Figure 16). In KITAHARA, a mid-portion 32 of each lead is formed to a circular-arc shape and pressed to fall into the window 44 (column 6, lines 21-23), but the outer end 33 never falls into window 44.

Thus, KITAHARA neither teaches nor suggests the above-recited features of the present invention concerning the location of the two ends of the leads. In view of the shortcomings of the reference, the pending rejections are further believed to be non-viable.

Moreover, as recited in claim 8, a gap between the insulation film and the wiring substrate is filled with resin, while a gap between the IC chip and the base is filled with resin in KITAHARA (see column 5, lines 53-58). Claim 8 has therefore been amended to recite that a gap between the solder balls is free of resin so as to further distinguish from the applied reference.

For all the reasons above, the anticipation and obvious rejections are both believed to be non-viable. Accordingly,

reconsideration and allowance of all the pending claims are respectfully requested.

In view of the foregoing remarks, applicant respectfully submits that all of the pending claims are in condition for allowance and an early indication of the same is respectfully requested.

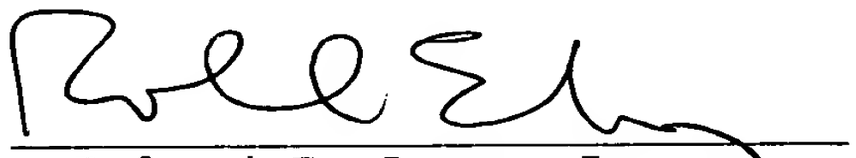
Should there by any matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Attached hereto is a marked-up version of the changes made to the specification and claims. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

YOUNG & THOMPSON

By 

Roland E. Long, Jr.
Attorney for Applicant
Registration No. 41,949
745 South 23rd Street
Arlington, VA 22202
Telephone: (703)521-2297

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 1, the last paragraph bridging pages 1 and 2, was amended as follows:

--With reference to Fig. [6] 7, in such a conventional semiconductor device, a semiconductor chip 21 and a wiring [substr te] substrate 25 are connected to each other by welded solder balls 26 of the semiconductor chip 21. Further, resin 29 is injected into the gap between the semiconductor chip 21 and the wiring substrate 25 so as to cover the solder balls 26. The resin 29 is injected for the purpose of alleviating the thermal stress caused by the difference in the coefficient of thermal expansion between the semiconductor chip 21 and the wiring substrate 25. The semiconductor chip 21 and the wiring substrate 25 repeat expansion and contraction by heat generated by operations (on/off operation) of the device. However, the coefficient of thermal expansion of the semiconductor chip 21 is about 3.5 ppm whereas the coefficient of thermal expansion of the wiring substrate 25 is about 16 ppm in case of a printed board and about 8 ppm in case of an alumina substrate. Due to this difference in the coefficient of thermal expansion between the semiconductor chip 21 and the wiring substrate 25, the solder balls 26 are alternately subject to compressive stress and tensile stress. As a result, the solder balls 26 are broken at an early stage due to thermal fatigue, which causes electric

disconnection, resulting in a signal transmission stop or a power supply stop.--

IN THE CLAIMS:

Claim 1 was amended as follows:

--1. (amended) A mounting structure of a semiconductor device comprising:

a semiconductor chip which is provided with a plurality of solder balls arranged in a grid array;

a wiring substrate which is provided with a plurality of connection pads; and

an insulating sheet which has a plurality of leads and which is provided between said semiconductor chip and said wiring substrate,

wherein said plurality of solder balls are electrically connected through said leads to corresponding ones of said connection pads, respectively.--

Claim 8 was amended as follows:

--8. (amended) The mounting structure of a semiconductor device as claimed in claim 4,

wherein the gap between said insulating sheet and said wiring substrate is filled with resin and a gap between solder balls is free of resin.--

Claim 14 was amended as follows:

--14. (amended) The insulating sheet as claimed in claim 13,

wherein said fixed one end of each of said leads [is connected] includes a portion shaped to receive by direct contact, a corresponding one of a plurality of solder balls of [said] a semiconductor chip, and said other end of each of said plurality of leads is [connected to] shaped to contact with a corresponding one of a plurality of connection pads of [said] a wiring substrate,

said portion being in contact with the first surface.--